and a second chopping signal to chop a differential input signal to said first amplification stage;

a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal and a level shifted second chopping signal to chop an output signal from said first amplification stage;

a first NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a first resistor;

a second NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to said clock signal to generate said second chopping signal and said level shifted second chopping signal across a second resistor; and

a clock generator circuit configured to generate said clock signal.

[c18] A circuit in accordance with Claim 17 fabricated on a silicon carbide substrate.

[c19] A circuit in accordance with Claim 17 further comprising at least one additional stage of amplification responsive to said chopped output signal from said first amplification stage.

[c20] A circuit in accordance with Claim 19 further comprising a sensor, wherein said first amplification stage is responsive to an output signal of said sensor chopped by said first NMOS depletion mode chopping switch.

[c21] A circuit in accordance with Claim 20 wherein said circuit and sensor are operated at a temperature in excess of 300 degrees Celsius.

[c22]

A method for amplifying a signal comprising:

generating an input signal;

amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal;

amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch that is responsive to a first chopping signal to produce a first chopped input signal; and

amplifying the first chopped input signal utilizing an NMOS depletion mode

amplifier stage to produce an amplified chopped output signal.

[c23] A method in accordance with Claim 22 wherein amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier, comprises chopping the amplified chopped output signal utilizing an NMOS depletion mode amplifier responsive to a level shifted first chopping signal to produce a chopper-stabilized output signal.

[c24] A method in accordance with Claim 23 further comprising generating, a opposite nodes of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal and the level shifted first chopping signal in response to a clock signal.